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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/605,716

10/21/2003

Li-Chun Tu

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11/07/2005

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION

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EXAMINER

MCFADDEN, MICHAEL B

ART UNIT

PAPER NUMBER

2188

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/605,716	TU ET AL.	
	Examiner	Art Unit	
	Michael B. McFadden	2188	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 October 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Priority***

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/605,716, filed on 12/10/2003.

### ***Drawings***

2. The drawings filed on 10/21/2003 are deemed acceptable by the examiner.

### ***Abstract***

3. The abstract filed on 10/21/2003 is deemed acceptable by the examiner.

### ***Specification***

4. The disclosure is objected to because of the following informalities:

In Section 7, Lines 9-11: The sentence does not read clearly. Please consider this as an appropriate substitute, "Accordingly, the stack memory is not adequate for complicated programs that need to call many subroutines".

In Section 7, Line 12: A space should be inserted between "of" and "subroutines". It should read, "Limited stack memory requires programs to call only a limited number of subroutines".

In Section 15, Line 1: "an" should be replaced with "the".

There are multiple inappropriate references to components of the drawings. All references to components of the drawings should be in parenthesis. This error occurs several times throughout the Specification and the Applicant's cooperation is requested in locating and correcting the errors. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 2 contains the trademark/trade name Micro Computer System® or MCS®. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade

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name is used to identify/describe a microcontroller and, accordingly, the identification/description is indefinite.

8. This claim will further be treated on its merits based on the changing of "Micro Computer System (MCS)®" to "microcontroller".

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Welfeld (U.S. Patent No. 6,167,047):

As per claim 1, Welfeld discloses a processor comprising:

A central processing unit (CPU) processing data according to an instruction set (Figure 5, element 130);

A data memory storing non-stack data (Figure 5, element 110 see column 8, lines 43-46);

A stack memory storing stack data (Figure 5, element 120 labeled Stack Memory, see column 9, lines 16-19);

A memory address generator producing addresses for accessing the data memory; and

A stack pointer generator producing pointers for accessing the stack memory;

The memory address generator and the stack pointer generator are inherently disclosed in Welfeld. Meaning that although the claimed elements are not expressly disclosed in the reference, they must be a part of the reference. In order to access memory addresses in the data memory there must be a memory address generator to provide the addresses used. Also, to be able to add and delete elements from the stack memory there must be a stack pointer generator to access the stack memory.

11. Claims 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Welfeld (U.S. Patent No. 6,167,047) and Microsoft Computer Dictionary (used as an evidentiary reference):

As per claim 2, Welfeld discloses the processor of claim 1 wherein the processor is a microcontroller (figure 5, element 100 see column 8, lines 30-32);

Although not expressly disclosed as such the Examiner respectfully asserts that the integrated circuit of Welfeld is a microcontroller.

A microcontroller is defined as a microprocessor on a single integrated circuit, which may also include small amounts of

memory, timers, and I/O ports (Microsoft Computer Dictionary, page 337).

It can then be seen that the integrated circuit of Welfeld includes a processor along with a programmable memory, a stack memory, a RAM arbiter, and a memory programmer all on a single integrated circuit, therefore, making it a microcontroller.

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Welfeld (U.S. Patent No. 6,167,047) as applied to claim 1 above, and further in view of Anderson et al. (hereinafter Anderson (U.S. Patent No. 3,969,724)).

As per claim 3, Welfeld fails to disclose the processor of claim 1 wherein the processor processes an 8-bit instruction set;

Anderson discloses the processor of claim 1 wherein the processor processes an 8-bit instruction set (Figure 1, element 10 and column 23, lines 1-2);

Welfeld and Anderson are analogous art because they are from the same field of endeavor, microprocessors;



At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the processor of Welfeld (Figure 5, element 130) with the central processing unit of Anderson (Figure 1, element 10;

The motivation for doing so would have been to perform data processing operations faster than before;

Therefore it would have been obvious to combine the central processing unit of Anderson with the integrated circuit of Welfeld in place of the processor (Figure 5, element 130) of Welfeld to perform data processing operations faster than before;

14. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welfeld (U.S. Patent No. 6,167,047) and Anderson (U.S. Patent No. 3,969,724) as applied to claim 3 above, and further in view of Shima et al. (hereinafter Shima (U.S. Patent No. 4,332,008)).

As per claim 4, Welfeld and Anderson fail to disclose the processor of claim 3 wherein the data memory is 256 bytes.;

Shima discloses the data memory that is 256 bytes (column 6, lines 15-18);

Welfeld, Anderson, and Shima are from analogous art because they are from the same field of endeavor, microprocessors;

At the time of invention it would have been obvious to a person of ordinary skill in the art to replace the programmable memory from Welfeld (Figure 5, element 110) with the data memory from Shima.



The motivation for doing so would have been that most computer systems require some amount of external Read/Write memory for data storage and to implement a "stack" (column 6, lines 15-17);

Therefore it would have been obvious to combine the data memory of Shima with the integrated circuit of Welfeld and Anderson to provide the external Read/Write memory, for data storage and implementing a "stack", that most computers require.

15. As per claim 5, Welfeld and Anderson fail to disclose the processor of claim 3 wherein the stack memory is 256 bytes.;

Shima discloses the stack memory that is 256 bytes (column 6, lines 15-18);

Welfeld, Anderson, and Shima are from analogous art because they are from the same field of endeavor, microprocessors;

At the time of invention it would have been obvious to a person of ordinary skill in the art to replace the stack memory from Welfeld (Figure 5, element 110) the stack memory from Shima.

The motivation for doing so would have been that most computer systems require some amount of external Read/Write memory for data storage and to implement a "stack" (column 6, lines 15-17);

Therefore it would have been obvious to combine the data memory of Shima with the integrated circuit of Welfeld and Anderson to provide the

external Read/Write memory, for data storage and implementing a "stack", that most computers require.

16. Shima is used for both claim 4 and claim 5 because the reference discloses both uses for the memory, data and stack, at the size specified. When the programmable memory and stack memory of Welfeld are replaced with the external Read/Write memory of Shima then both memories are 256 bytes as specified in claims 4 and 5.

### ***Conclusion***

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tu et al. (U.S. Patent Publication No. US 2004/0172516) discloses a processor where an extended memory is used to exclusively store stacks and the original memory is reserved for data.

Poisner et al. (U.S. Patent No. 6,938,153) discloses a CPU stack that is located in memory separate from the main memory.

Chaudhry et al. (U.S. Patent No. 6,430,649) discloses a main memory partitioned between a stack and a heap.

Banning et al. (U.S. Patent No. 6,615,300) discloses a RAM array separate from the main memory that logically divided the RAM array into two sections: a memory stack and a cache.

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18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. McFadden whose telephone number is (571)272-8013. The examiner can normally be reached on Monday-Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBM

*Mano Padmanabhan*  
10/31/05

**MANO PADMANABHAN**  
**SUPERVISORY PATENT EXAMINER**